

WHAT IS CLAIMED IS:

1. A level shifter for changing an input signal whose level changes between a first voltage level and a ground voltage level into an output signal whose level changes between a second voltage level and the ground voltage level, the level shifter comprising:

a first input transistor and a second input transistor which receive the input signal and an inversion signal of the input signal, respectively;

a first load transistor and a second load transistor, one side of each transistor being connected to the second voltage level;

10 a first switch transistor connected between the first load transistor and the first input transistor, the first switch transistor responds to the inversion signal;

a second switch transistor connected between the second load transistor and the second input transistor, the second switch transistor responds to the input signal;

15 a first output unit that generates the output signal in response to a signal generated at a connection node between the first load transistor and the first switch transistor and a signal at a connection node between the first input transistor and the first switch transistor; and

a second output unit that generates a complementary signal of the output signal in response to a signal generated at a connection node between the second load transistor and the second switch transistor and a signal at a

connection node between the second input transistor and the second switch transistor.

2. The level shifter of claim 1, wherein the first and second input
5 transistors are NMOS transistors.

3. The level shifter of claim 1, wherein the first and second load transistors are PMOS transistors.

10 4. The level shifter of claim 3, wherein a gate of the first load transistor is connected to the connection node between the second input transistor and the second switch transistor, and a gate of the second load transistor is connected to the connection node between the first input transistor and the first switch transistor.

15 5. The level shifter of claim 1, wherein the first and second switch transistors are PMOS transistors.

20 6. The level shifter of claim 1, wherein the first output unit comprises a PMOS transistor and an NMOS transistor connected in serial between the second voltage level and the ground voltage level,

wherein a signal generated at the connection node between the first load transistor and the first switch transistor is applied to a gate of the PMOS transistor, a signal generated at the connection node between the first input transistor and the first switch transistor is applied to a gate of the NMOS transistor, and the output signal is output from a connection node between the PMOS transistor and the NMOS transistor.

7. The level shifter of claim 1, wherein the second output unit comprises a PMOS transistor and an NMOS transistor connected in serial between the second voltage level and the ground voltage level,

wherein a signal generated at a connection node between the second load transistor and the second switch transistor is applied to a gate of the PMOS transistor, and a signal at a connection node between the second input transistor and the second switch transistor is applied to a gate of the NMOS transistor, the complementary signal of the output signal is output from a connection node between the PMOS transistor and the NMOS transistor.

8. A level shifter for changing an input signal whose level changes between a first voltage level and a ground voltage level into an output signal

whose level changes between a second voltage level and the ground voltage level, the level shifter comprising:

first through fourth nodes;

5 a first PMOS transistor comprising a source, a drain, and a gate connected to the second voltage level, the first node, and the fourth node, respectively;

a second PMOS transistor comprising a source, a drain, and a gate connected to the first node, the second node, and an inversion signal of the input signal, respectively;

10 a first NMOS transistor comprising a drain, a source, and a gate connected to the second node, the ground voltage level, and the input signal, respectively;

a third PMOS transistor comprising a source, a drain, and a gate connected to the second voltage level, the third node, and the second node, respectively;

15 a fourth PMOS transistor comprising a source, a drain, and a gate connected to the third node, the fourth node, and the input signal, respectively;

a second NMOS transistor comprising a drain, a source, and a gate connected to the fourth node, the ground voltage level, and the inversion signal of the input signal, respectively;

20 a fifth PMOS transistor comprising a source, a gate, and a drain connected to the second voltage level, the first node, and an output node, respectively;

a third NMOS transistor comprising a drain, a gate, and a source connected to the output node, the second node, and the ground voltage level, respectively;

5 a sixth PMOS transistor comprising a source, a gate, and a drain connected to the second voltage level, the third node, and a complementary output node, respectively; and

a fourth NMOS transistor comprising a drain, a gate, and a source connected to the complementary output node, the fourth node, and the ground voltage level, respectively.

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9. The level shifter of claim 8, further comprising an inverter for using the first voltage level as a power source, inverting the input signal, and outputting the inversion signal of the input signal.